Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously presented). An improved ISDN-data transmission method for transmitting digital data divided up into HDLC data frames of variable lengths from a first data bus to a second data bus operated asynchronously with respect to the first data bus and controlled by a microprocessor, the improvement which comprises:

writing the digital data of a given HDLC-data frame from the first data bus to a memory having a settable size, said memory being arranged directly between said first data bus and said second data bus;

informing the microprocessor, in a form of an interrupt signal generated by a memory control unit, if the memory is full or if the memory contains an entry indicating an end of a respective HDLC-data frame;

determining via the microprocessor from the memory control unit a quantity of the digital data to be read from the memory;

reading via the microprocessor the digital data from the memory;

setting dynamically via the microprocessor a size of the memory for a current reading/writing procedure of said memory; and

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transmitting from the microprocessor to the memory control unit an acknowledgment of a reception of the data being read out from the memory.

Claim 2 (original). The method according to claim 1, which comprises supplying the digital data from the first data bus to a high-level data link control logic unit which checks whether the digital data has been received correctly before the digital data is written to the memory.

Claim 3 (previously presented): An improved ISDN-data transmission method for transmitting digital data divided up into HDLC data frames of variable lengths from a first data bus, controlled by a microprocessor, to a second data bus operated asynchronously with respect to the first data bus, the improvement which comprises:

writing the digital data from the first data bus to a memory having a settable size, said memory being arranged directly between said first data bus and said second data bus;

performing one of informing the microprocessor, in a form of an interrupt generated by a memory control unit, if the memory is ready to accept new data from the first data bus, and the microprocessor asking the memory control unit if the memory is ready to accept the new data from the first data bus;

writing via the microprocessor the new data to the memory;

setting dynamically via the microprocessor a size of the memory for a following reading/writing procedure of said memory, the settable size being dependent on the size of said transmitted HDLC-data frame being written at the same time in said memory;

transmitting from the microprocessor to the memory control unit an acknowledgment of the data being written into the memory; and

placing the new data onto the second data bus.

Claim 4 (original). The method according to claim 3, which comprises supplying the new data to a high-level data link control logic unit before it is placed onto the second data bus, the high-level data link control logic unit adding error-checking data to the new data.

Claim 5 (currently amended). A configuration for performing an ISDN-data transmission method for transmitting digital data divided up into HDLC data frames of variable length from a first data bus to a second data bus operated asynchronously with respect to the first data bus and controlled by a microprocessor, the configuration comprising:

a memory having a settable size for storing data received from the first data bus and for subsequently reading out by the microprocessor, said memory being arranged directly between said first data bus and said second data bus, the settable size being dependent on the size of said transmitted HDLC-data frame being written at the same time in said memory;

a control device for controlling access operations to said memory by the first data bus and the microprocessor;

a first register storing an amount of the data being currently written in the memory and currently read out ~~from~~ by the microprocessor; and

a second register storing, for a following writing procedure, a present size of memory, said second register having a content selectively modifiable with each read cycle of the microprocessor.

Claim 6 (original). The configuration according to claim 5, including a high-level data link control HDLC logic unit connected between the first data bus and said memory.

Claim 7 (previously presented). The configuration according to claim 5, wherein the memory comprises a FIFO.

Claim 8 (previously presented). The method according to claim 1, wherein the memory comprises a FIFO.

Claim 9 (currently amended). The method according to claim 3, wherein the memory comprises a ~~FIFOuj~~ FIFO.